IN THE CLAIMS

Following are the claims as currently pending for consideration.

1. (Original) An apparatus comprising:

multiprocessing circuitry to provide a plurality of processing elements;

a machine check abort handling mechanism to quiet the plurality of processing elements in response to a machine check abort exception condition, and to permit at least one processing element of the plurality of processing elements to execute a first exception handler responsive to the machine check abort exception condition and to attempt a recovery.

2. (Original) The apparatus of Claim 1 wherein the machine check abort handling mechanism permits a second processing element of the plurality of processing elements to continue execution responsive to the attempted recovery of said at least one processing element being a success.

3. (Original) The apparatus of Claim 1 wherein the plurality of processing elements are quieted by permitting scheduled operations to complete.

4. (Original) The apparatus of Claim 3 wherein the scheduled operations are permitted to complete as a result of each the plurality of processing elements executing a HALT instruction.

5. (Original) The apparatus of Claim 1 which, wherein the machine check abort handling mechanism permits a second processing element to execute a second exception handler responsive to the identified machine check abort exception condition.

6. (Original) The apparatus of Claim 5 wherein the execution of the first exception handler by said at least one processing element is mutually exclusive to the execution of the second exception handler by the second processing element.

7. (Original) The apparatus of Claim 6, wherein the machine check abort handling mechanism synchronizes said at least one processing element and the second processing element responsive to the attempted recovery of said at least one processing element being a success.

8. (Original) The apparatus of Claim 6 wherein the mutually exclusive execution is accomplished through use of a semaphore.

9. (Original) The apparatus of Claim 6 wherein the identified machine check abort exception condition involves a resource shared by said at least one processing element and said second processing element.

10. (Original) The apparatus of Claim 9, wherein said at least one processing element and said second processing element arbitrate for access to the shared resource.

11. (Original) An apparatus comprising:

multiprocessing circuitry to provide a plurality of processing elements;

a machine check abort handling mechanism to quiet the plurality of processing elements responsive to a machine check abort exception condition;

a first processing element of the plurality of processing elements to attempt a recovery responsive to the machine check abort exception condition; and

a second processing element of the plurality of processing elements to continue execution responsive to the attempted recovery of the first processing element being a success.

12. (Original) The apparatus of Claim 11 wherein the processing elements are quieted as a result of each the plurality of processors executing a HALT instruction.

13. (Original) The apparatus of Claim 11 wherein the second processor is also to attempt a second recovery responsive to the machine check abort exception condition.

14. (Original) The apparatus of Claim 13 wherein the first processor and the second processor synchronize responsive to a success with respect to the attempted recovery of the first processing element.

15. (Original) The apparatus of Claim 13 wherein the attempted recovery of the first processing element is mutually exclusive to the attempted second recovery of the second processing element.

16. (Original) The apparatus of Claim 15 wherein the mutually exclusive attempted recoveries are accomplished through use of a semaphore.

17. (Original) The apparatus of Claim 15 wherein the machine check abort exception condition involves a resource shared by the first processing element and the second processing element.

18. (Original) The apparatus of Claim 17 wherein the first processor and the second processor arbitrate for access to the shared resource.

19. (Original) A system comprising:

multiprocessing circuitry to provide a plurality of processing elements;

communication circuitry to signal the plurality of processing elements to quiet activity, said signal being responsive to a machine check abort exception condition; and

one or more storage medium accessible at least to a first processing element of the plurality of processing elements, said one or more storage medium having an executable exception handler stored thereon, which, when accessed by the first processing element, causes the first processing elements to check error conditions responsive to the machine check abort exception condition, and to attempt a recovery.

20. (Original) The system of Claim 19 further comprising:

a synchronization mechanism to permit the plurality of processing elements to continue execution if said attempted recovery is a success.

21. (Original) The system of Claim 20 wherein the synchronization mechanism is further to arbitrate among the plurality of processing elements for access to a shared resource.

22. (Original) The system of Claim 21 wherein the synchronization mechanism comprises a semaphore control mechanism.

23. (Original) The system of Claim 19 wherein the communication circuitry comprises a broadcast network to broadcast the machine check abort exception condition to signal the plurality of processing elements.

24. (Original) The system of Claim 19 being fabricated on a single die.

25. (Original) The system of Claim 19 wherein the plurality of processing elements may have mutually exclusive access to the executable exception handler to provide mutually exclusive handling of the machine check abort exception condition.

26. (Original) A system comprising:

multiprocessing circuitry to provide a plurality of processing elements;

communication circuitry to signal the plurality of processing elements to quiet

activity, said signal being responsive to a machine check abort exception condition; and

a synchronization mechanism to permit the first plurality of processing elements to continue activity upon a successful recovery from the machine check abort exception condition.

27. (Original) The system of Claim 26 further comprising one or more storage medium having an executable code stored thereon which, when executed by one or more of the plurality of processing elements, causes the one or more of the plurality of processing elements to check error conditions responsive to the machine check abort exception condition, and to attempt a recovery.

28. (Original) The system of Claim 27 wherein the identified machine check abort exception condition involves a resource shared by two or more of the plurality of processing elements.

29. (Original) The system of Claim 27 wherein the executable code comprises an executable exception handler and the plurality of processing elements may have mutually exclusive access to the executable exception handler to check error conditions responsive to the machine check abort exception condition, and to attempt the recovery.

30. (Original) The system of Claim 26 being fabricated on a single die.